CodeWarriors & Processor Expert Seminar

AMF-GEN-T0011

CodeWarriors IDE and Processor Expert In-depth Training Presented by Hy Mai and Ruth Rhoades

- ► How to position and sales Processor Expert
- ►LAB1 -- Blinking LED (Timer and I/O)
- ►LAB2 KBI & Analog Compartor
- ►LAB3 -- ADC and PWM
- ► LAB4 SCI (Uart) Communication with PC
- ► LAB5 SPI Serial Peripheral Comm neighbor's board
- ► LAB6 I2C Comm with neighbor's board
- ►LAB7 Input Capture to measure Pulsewidth (Optional)
- ►LAB8 Make check payable to He My FAE

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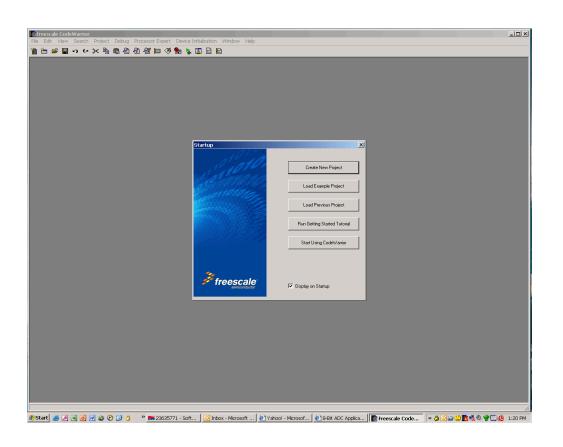


- ► Configure Bus Clock to 8Mhz
- ► Set Timer to generate an interrupt every 250ms
- ► Configure output on LED2 (PORTB7)
- ► Toggle LED at every Timer Interrupt



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•Click "Create New Project"

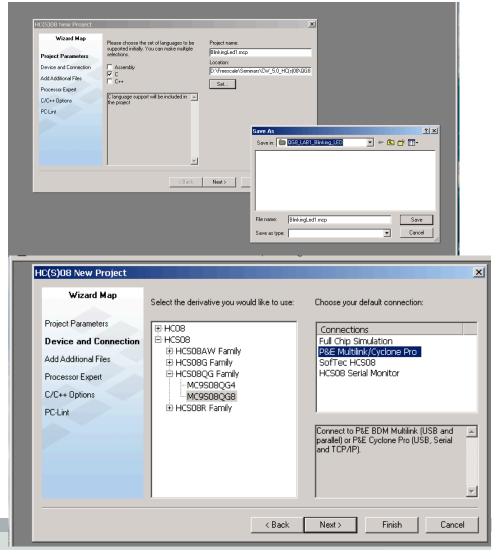


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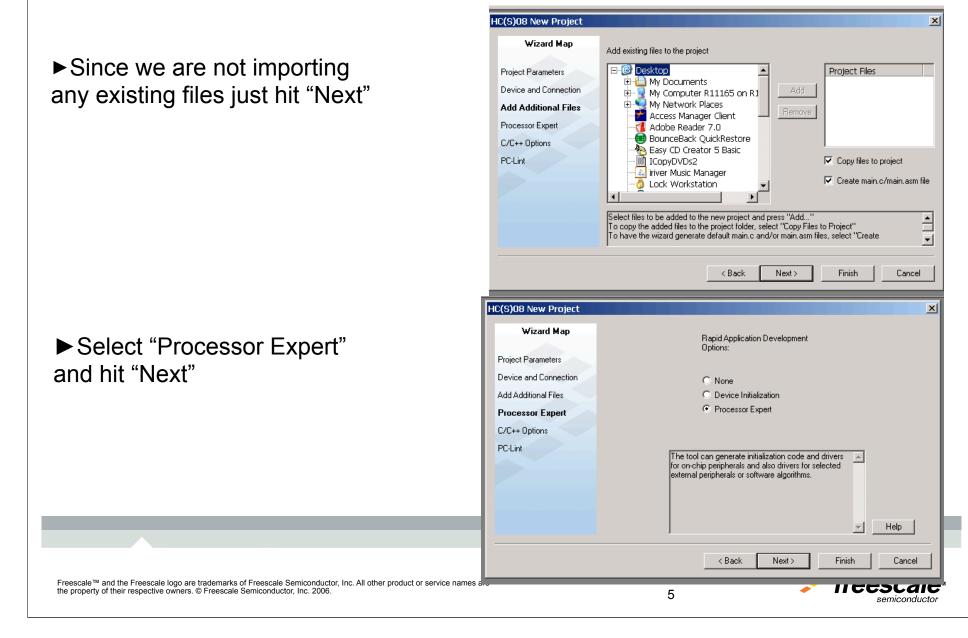
Click on the "Set" button to set the directory
Give the project a name and hit "Save" and then hit "Next"

Expand the "HCS08" directory structure to and find the "MC9S08QG8" device
Select "P&E Multilink/Cyclone Pro" under the Connections box, then hit "Next"



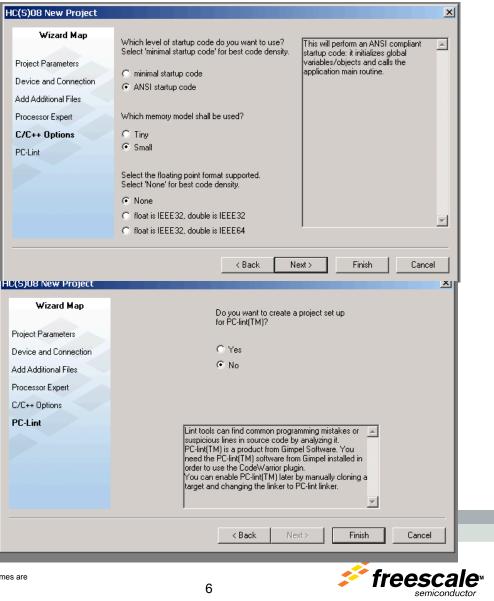
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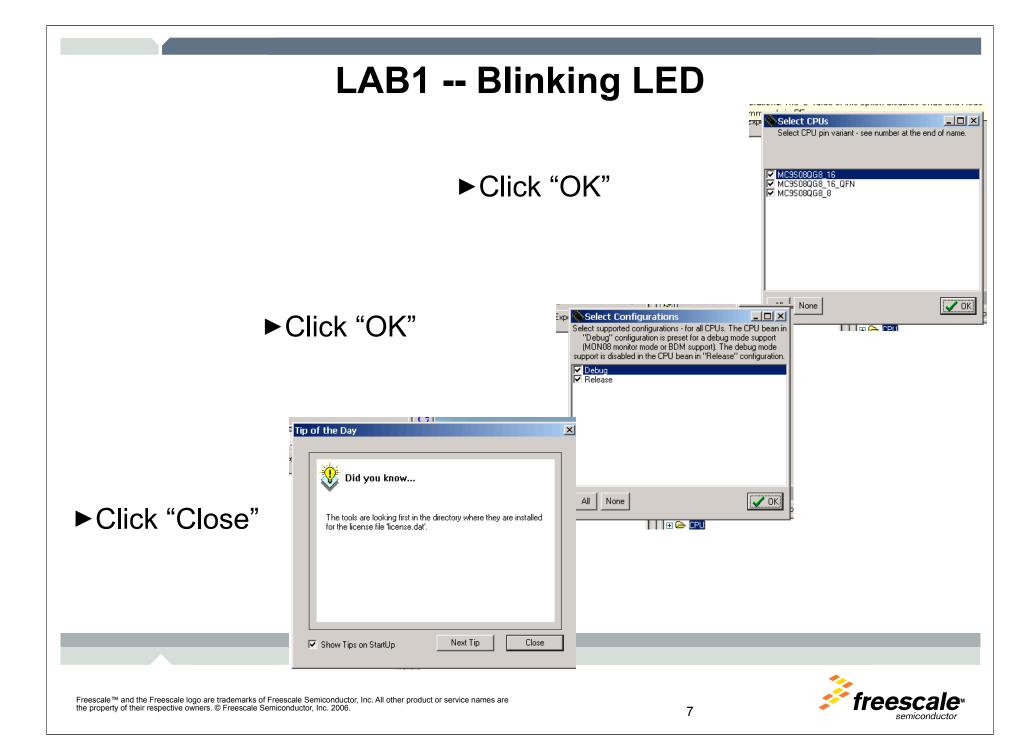


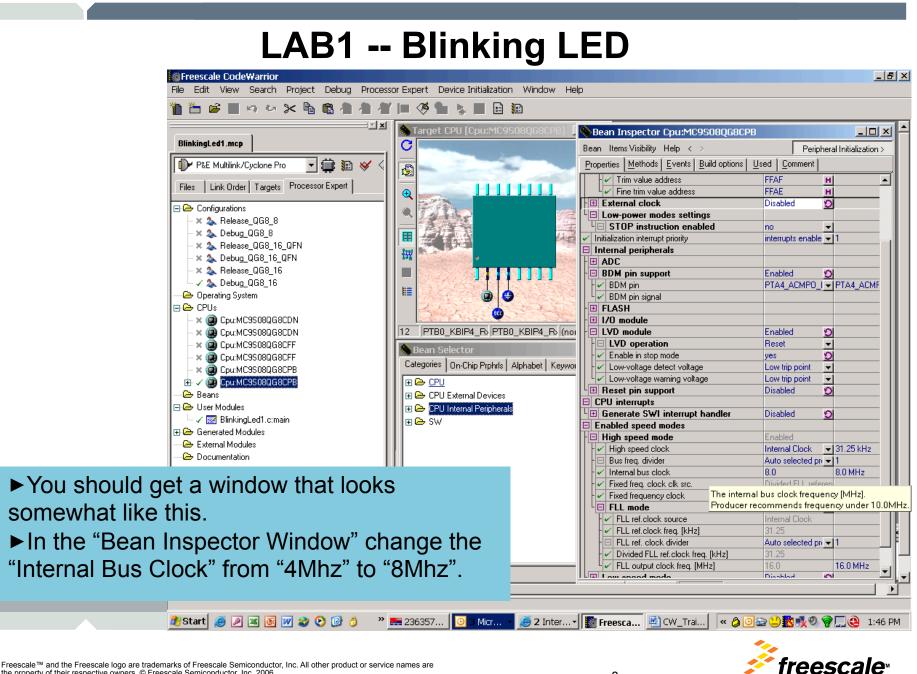
Leave everything as default and click "Next"

Leave everything as default and click"Finish"



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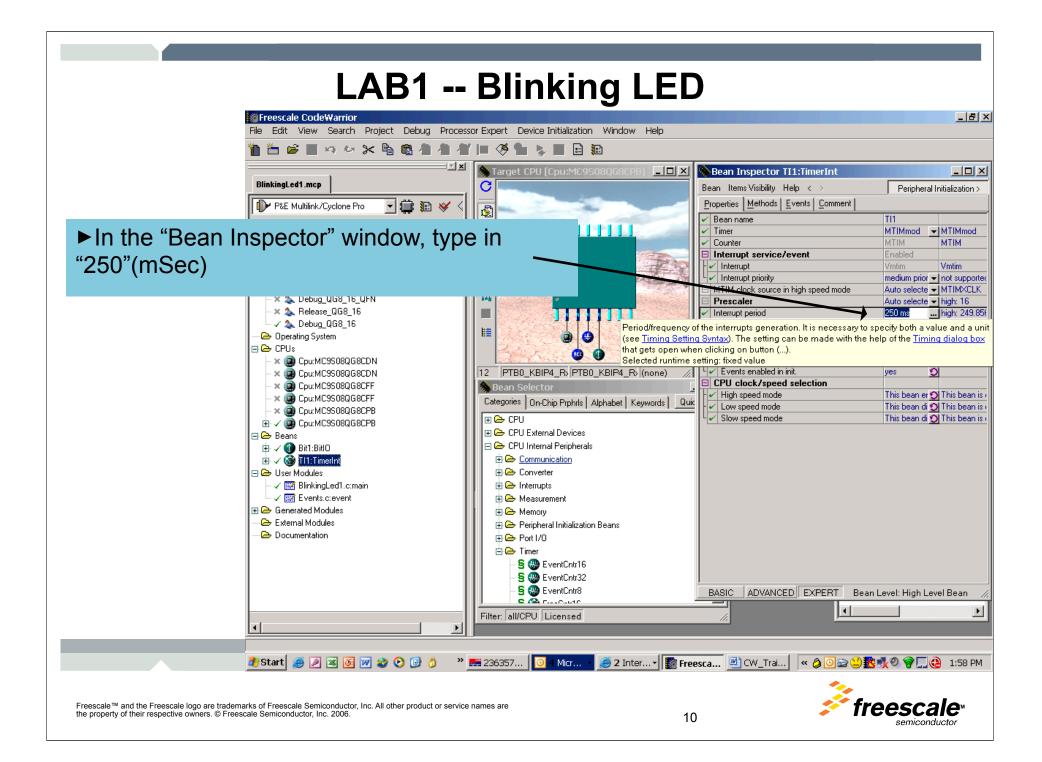


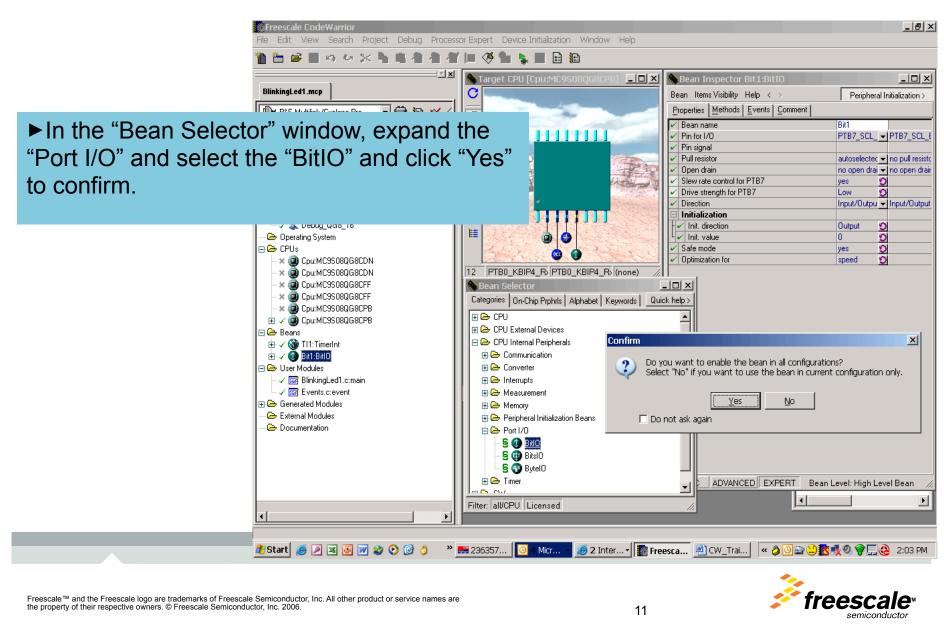


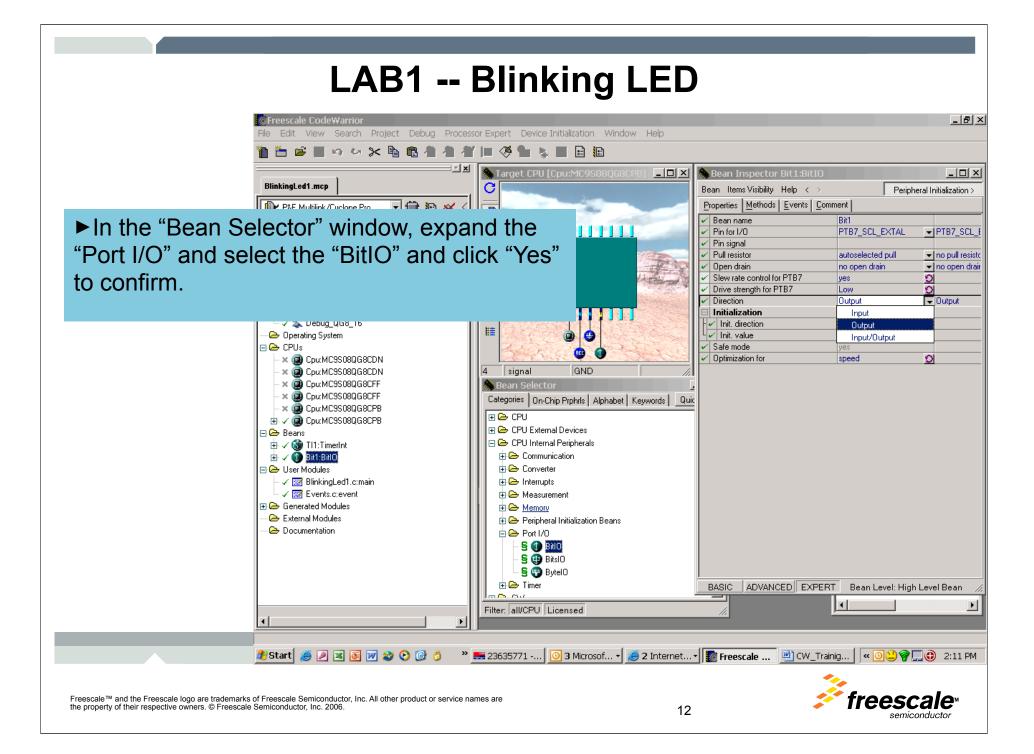
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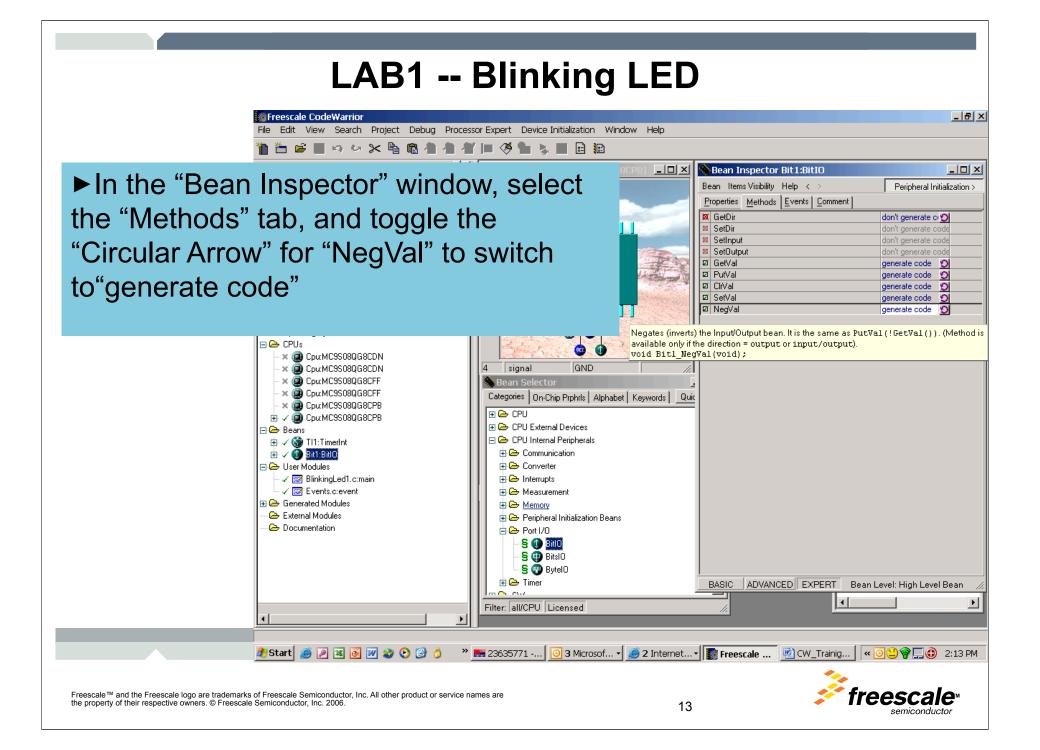
Freescale CodeWarrior - 리 × File Edit View Search Project Debug Processor Expert Device Initialization Window Help 🖻 📕 🗠 🗠 🔀 🐴 🛍 🐴 1 i 🖉 🐂 💺 🔳 🖻 🔢 1 arget CPU [Cpu:MC9S080 - U × Ѧ Bean Inspector TI1:TimerInt - 🗆 × BlinkingLed1.mcp С Bean Items Visibility Help < > Peripheral Initialization > Properties Methods Events Comment P&E Multilink/Cyclone Pro - 🗰 🔝 ~ 6 🖌 Bean name TI1 Files Link Order Targets Processor Expert ~ V Timer MTIMmod - MTIMmod _ 🗆 🗙 iter MTIM MTIM Bean Selector 🖃 🗁 Configurations Irrupt service/event Enabled Categories On-Chip Prphrls Alphabet Keywords Quick help > 🗶 🏡 Release_QG8_8 Vmtim rrupl 🗶 為 Debug QG8-8 🗊 🗁 CPU errupt priority medium prior - not supported 🗶 🏡 Release_QG8_16_QFN 🕀 🗁 CPU External Devices I clock source in high speed mode Auto selecte - MTIMXCLK 🗶 🏡 Debug_QG8_16_QFN 🖃 🗁 CPU Internal Peripherals caler Auto selecte 👻 high: not set 🛪 🏊 Release_QG8_16 ... Unassigned I upt period 🕂 🗁 Communication 🗸 為 Debug_QG8_16 e period in modes O yes 🕂 🗁 Converter - 🗁 Operating System i uses entire timer Ð no 🕂 🗁 Interrupts 🖃 🗁 CPU 🛚 alization 🗄 🗁 Measurement abled in init, code Ð 🗶 🍘 Cpu:MC9S08QG8CDN yes 🕂 🗁 Memory ents enabled in init. 0 🛪 🍘 Cpu:MC9S08QG8CDN yes 🗄 🗁 Peripheral Initialization Beans clock/speed selection 🗶 🍘 Cpu:MC9S08QG8CFF 🕂 🗁 Port I/O h speed mode This bean er 🕥 This bean is 🛛 - 🗶 🍘 Cpu:MC9S08QG8CFF This bean di 🕥 This bean is (🕂 🗁 Timer w speed mode 🗶 🍘 Cpu:MC9S08QG8CPB This bean di 🕥 This bean is 🛛 w speed mode S 🛞 EventCntr16 🗄 🗸 🍘 Cpu:MC9S08QG8CPB 🧧 🛞 EiventChtr32 🖃 🗁 Beans S 💮 EventCntr8 🗄 🗸 🌒 Bit1:BitlO 🛨 🍸 🛞 TI1:TimerInt 🗧 🚳 FreeCntr16 Confirm × 🖃 🗁 User Modules 🧧 🚳 FreeCntr32 🗸 🔣 BlinkingLed1.c:main S 🚳 FreeCntr8 Do you want to enable the bean in all configurations? ? - 🗸 🔜 Events.c:event 🧧 🐽 PPG. Select "No" if you want to use the bean in current configuration only. 🕀 🗁 Generated Modules S 💿 PWM - 😂 External Modules S 🚳 RTIshared <u>N</u>o. - 🗁 Documentation Yes 🗧 🚇 TimeDate S 🛞 TimerInt 🔲 Do not ask again 🧧 🕕 TimerOut 🧧 🕄 WatchDog 🕀 🗁 🕀 ► In the "Bean Selector" window, expand the Filter: all/CPU Licensed "CPU Internal Peripherals", "Timer", and select • the "TimerInt" bean. Then Click "Yes" to 🥶 2 Inter... -ಶ Start 🥭 🔎 🗷 💽 😿 🍪 🕑 🚱 👌 » 🔜 236357... Micr... confirm. Freescale ™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service n the property of their respective owners. © Freescale Semiconductor, Inc. 2006.

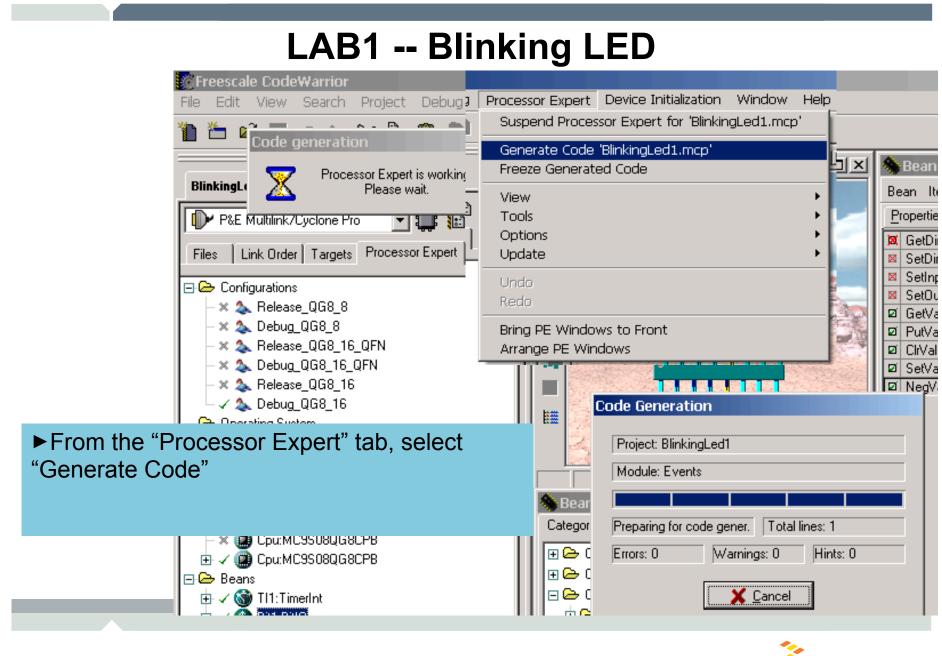
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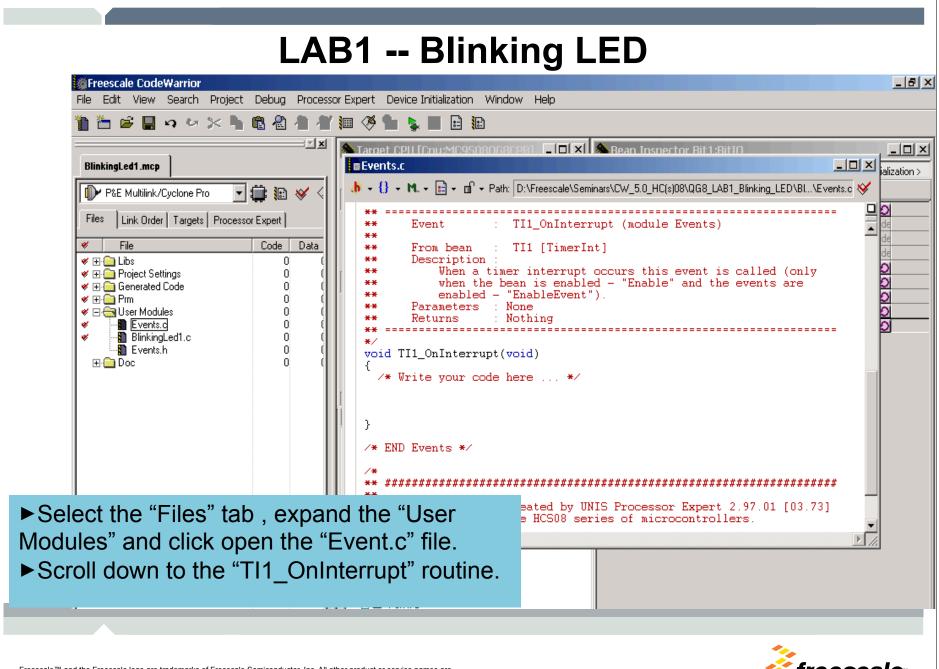






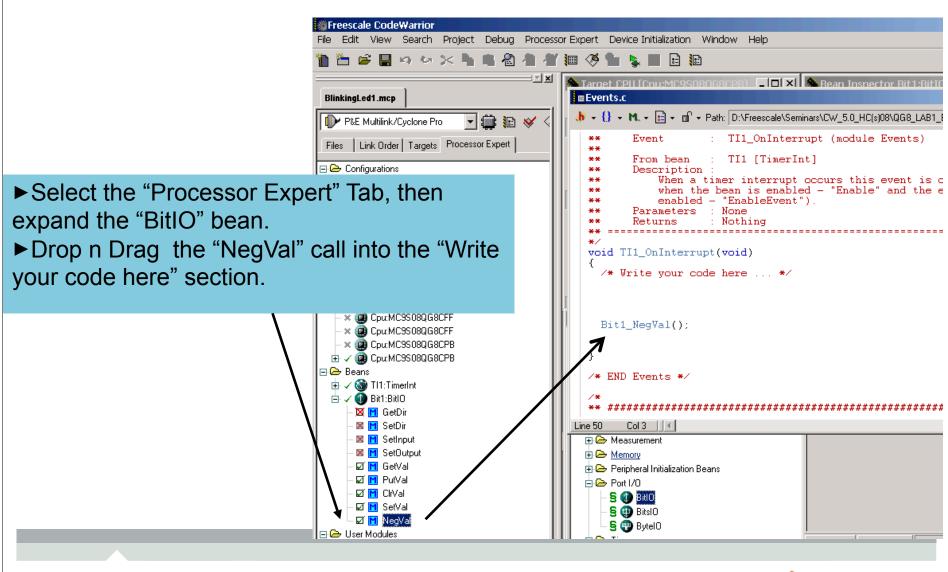
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LAB1 Blinking LED
File Edit View Search Project Debug Processor Expert Device Initialization Window Help
BlinkingLed1.mcp
P&E Multilink/Cyclone Pro 🔄 🌐 🌆 🎸 🌺 📗 🔸 🦉 🏊 🔤 🖓 🖓 🖓 Ru + 🖻 + 🗗 + Path: D:\Freescale\Seminars\CW_5.0_HC(s)08\QG8_LAB1_Blinking_LED\BL\Events.c
Files Link Order Targets Processer Ext Debug The Event TT1_On Internment (nodulo Events) Files Link Order Targets Processer Ext Imment of the second se
File View Run MultilinkCyclonePro Component Memory Window Help
► Hit the "Debug" Icon, and then click
You have selected to display this dialog on startup. Specify communications
► Click "Yes" to load image to Flash
Interface: USB HCS08/HCS12 Multilink - USB Port Add LPT Port
- × (2) Cpu:MC9508QG8CDN - × (2) Cpu:MC9508QG8CFF Port: DEM09508QG8 on USB1 (Name=PE5122327) (Autodetected)
- × Cpu:MC9508QG8CFF
E V 🙆 Cpu:MC9S08QG8CPB
□ ⊡ Beans CPU: HCS08 Processor - Autodetect
Erase and Program Flash?
It and before communicating to target for 0 milliseconds (decimal)
Load image contains flash memory data. Erase and Program flash?
Helay Control [Voltage -> Power-Uut Jack]
Yes No Preadys Hegulator Utiput Voltage Power Up Delay 2.00 ms .upon software exit 5V Power Up Delay 250 ms Image: Comparison of the second s
□ Image: Description □ Image: Description □ Image: Vertical Action □ Image: Description
For Help, press F1
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LAR1 Plinking LE	ח ח
LAB1 Blinking LE	
Front TI1 On Internuet Tue-Time Simulator & Real-Time Debugger D:\Freescale\Seminars\CW	
File View Run MultilinkCyclonePro Component Memory Window Help	
Source Start/Continue (F5)	Assembly
D:\Freescale\Seminars\CW_5.0_HC(s)08\QG8_LAB1_Blinking_LED\Blin Line: 38	main
{ 🕨 🔺 /*** Processor Expert internal initialization. DON'T REM(EOFD JSR 0xE02D E100 BRA *+0 ;abs = 0xE100
<pre>PE_low level_init();</pre>	E102 BRSET 0,0x00,*+2 ;abs = (
/*** End of Processor Expert internal initialization.	E105 STX ,X
/* Write your code here */	
For evemple: for() () */	Register
Procedure	Auto
N Lit "Otart" ican to run the preservers	HX E100 SP BF
► Hit "Start" icon to run the program.	SR 6A Status VHINZC
► You should see a blinking LED	Memory
	Auto
	0080 C7 18 26 A6 80 C7 18 25% 🛋
	0088 81 87 C6 18 25 A4 40 27%.0'
Data:2	Command
main Auto Symb Local	Breakpoint
	in> 🔹
Start/Continue program Automatic (triggers, breakpoints, watchpoints, and tr	race possible) 9508QG8 ICD Bre /
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LAB 2 – KBI & ACMP

- ► Initialized KBI on SW2(PORTA3)
- ► Use SW2 to toggle LED1(PORTB6).
- Initialized Analog Comparator
- ► To use Photolight sensor to toggle LED2(PORTB6)



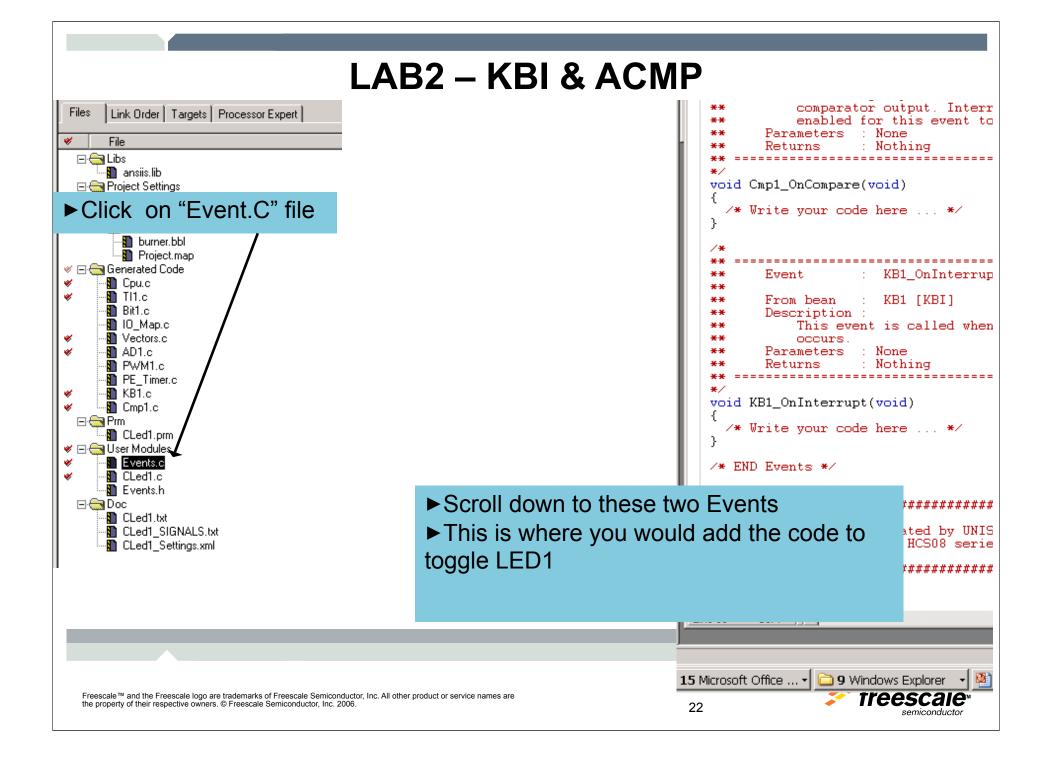
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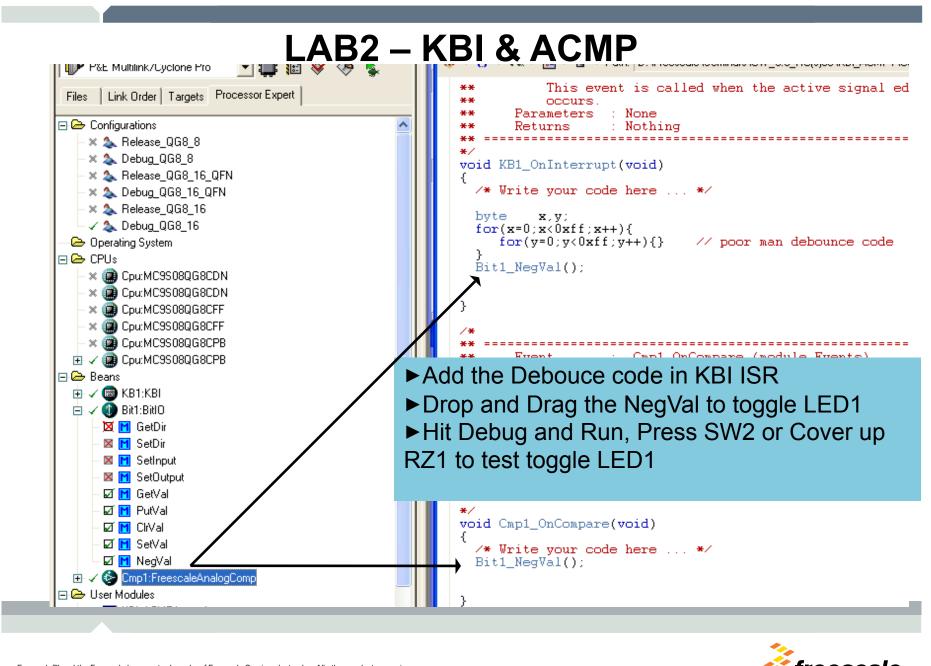
LAB2 – KBI & ACMP

rrors & Warnings	Sean Inspector KB1:KBI						
	Bean ItemsVisibility Help < >		Pe				
Categories On-Chip Prphrls Alphabet Keywords Quick help >	Properties Methods Events Comment						
🕀 🗁 CPU	✓ Bean name	KB1					
👔 🕀 CPU External Devices	✓ KBI		KBI				
, 🛛 🖻 🗁 CPU Internal Peripherals		1 + -					
🗄 🕀 Communication	Pin0						
🕀 🗁 Converter	Pin	PTA3_KBIP3_SCL_ADP3	PTA3_KBIP3_SCL_A				
E 🗁 Interrupts	V Pin signal	~ ~					
🝷 🚽 — 🗟 🌖 Extint	□ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	no 🖸	i Level en				
📕 🚽 S 🜐 InterruptVector	Pull resistor Generate interrupt on		pull up falling edge				
👽 🚽 S 🚳 🔀 🤾	Interrupt service/event	Enabled	naliing euge				
{ 🕀 🗁 Measurement		Vkeyboard	v Vkeyboard				
🕀 🗁 Memory <mark>Keyboard</mark>	V Interrupt priority		not supported				
 	Initialization						
Port I/O Port I/O	🛛 🖓 Enable in init. code	yes 💋	8				
🕀 🗁 Timer	└ ✓ Events enabled in init.	yes 🖸	8				
. 🕀 🗁 <u>SW</u>							
		·					
► From the "Bean Selector" click on "KBI" bean							
►Configure the Pin 0 for the KBI to be "PTA3_KBIP3_SCL_ADP3"							
Select "Pull Up" and "fallling edge" op	tions						
Make sure that Interrupts service is "Enabled"							
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the property of their respective owners. © Freescale Semiconductor, Inc. 2006.	20	✓ // C	escale ^M				

LAB2 – KBI & ACMP

Errors 2. Warnings Bean Selector Categories On-Chip Prphrls Alphabet Keywords Quick help > Construction Communication Communication Construction Click on "FreescaleAnalogCor	Bean Inspector Cmp1:F Bean Items Visibility Help < Properties Methods Events Bean name Analog comparator. Interrupt service/event Interrupt Mp" bean	>	Comp Cmp1 ACMP Enabled Vacmp medium priority	✓ ACMP ✓ ACMP ✓ Vacmp ✓ not supporter
 Measurement S Capture S FreescaleAnalogComp Memory Peripheral Initialization Beans Port I/O Timer SW 	✓ Fin ✓ Signal ✓ Pin ✓ Signal ⊡ Comparator output ✓ Analog comp. mode □ Initialization ✓ Enabled in init. code		VoltageReference PTA1_KBIP1_ADP1_AC Disabled falling edge yes	
 Configure "Analog comp mode to "fallin" Make sure that Interrupts service is "Er Click on "Generate Code" 	nabled"	Suspen		
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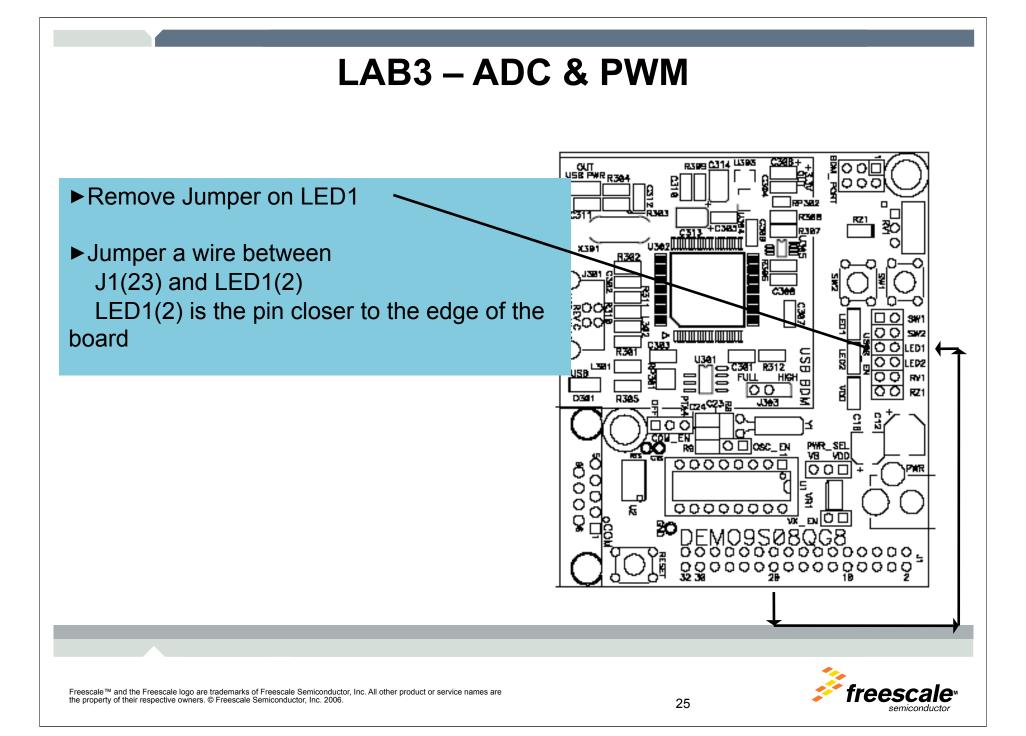
LAB3 – ADC & PWM

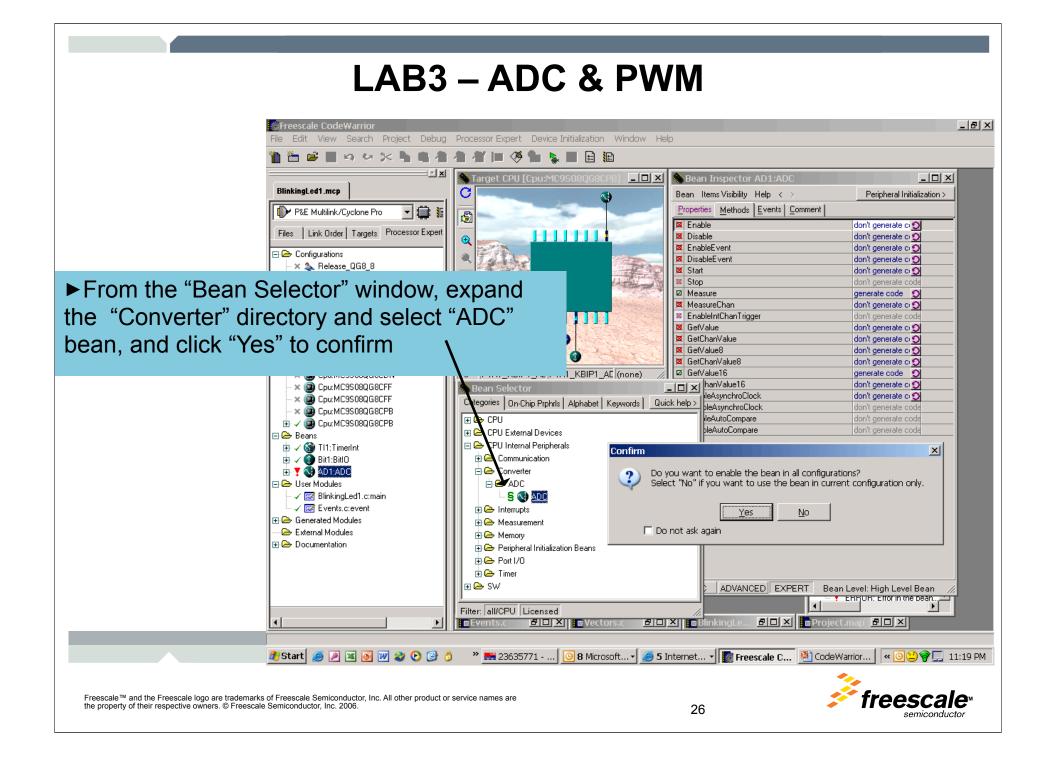
► Initialize ADC Channel 0 (PORTA0 –Potentiometer)

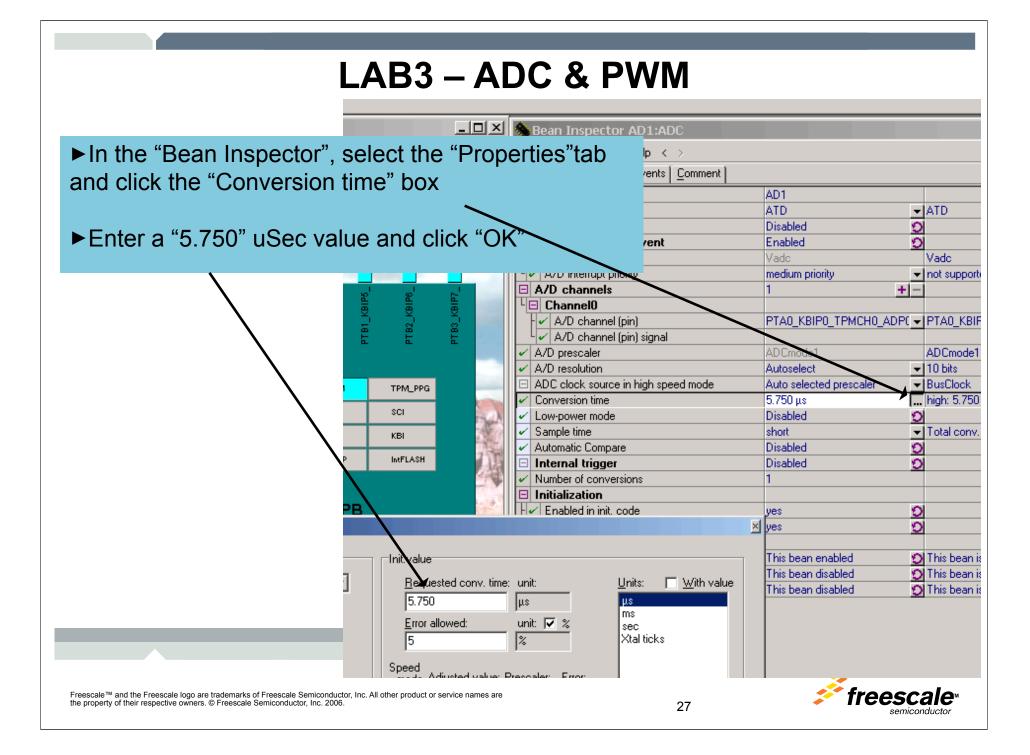
- ► Initialize PWM for 1mSec period with 64uSec initial on Pulse.
- ► Use ADC reading to reconfigure PWM ratio (duty cycle).
- ► Re-route PWM output to an LED1 to show dimming effect.

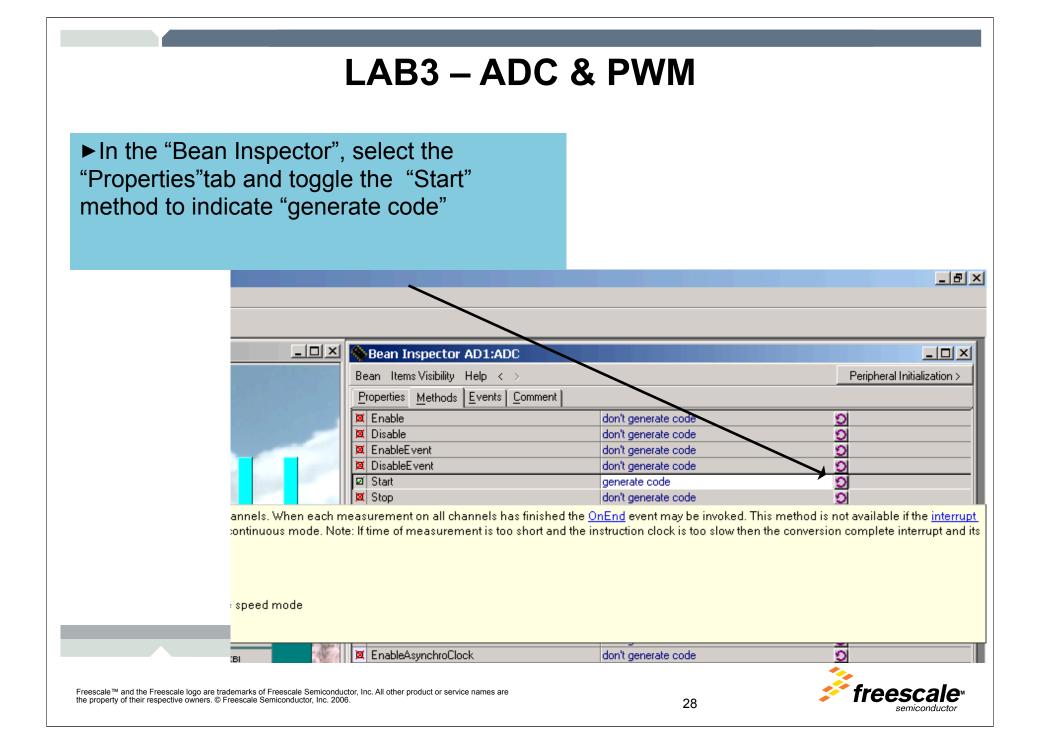


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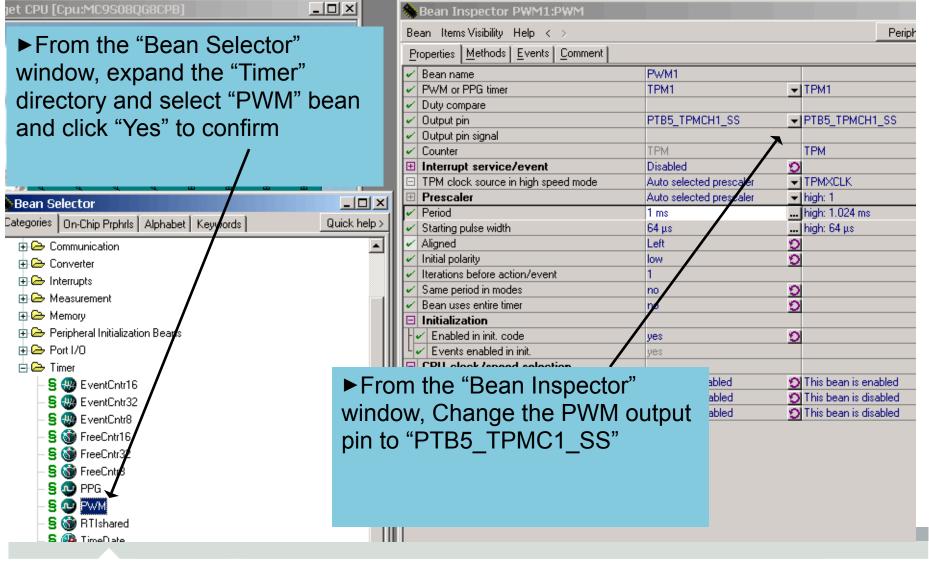








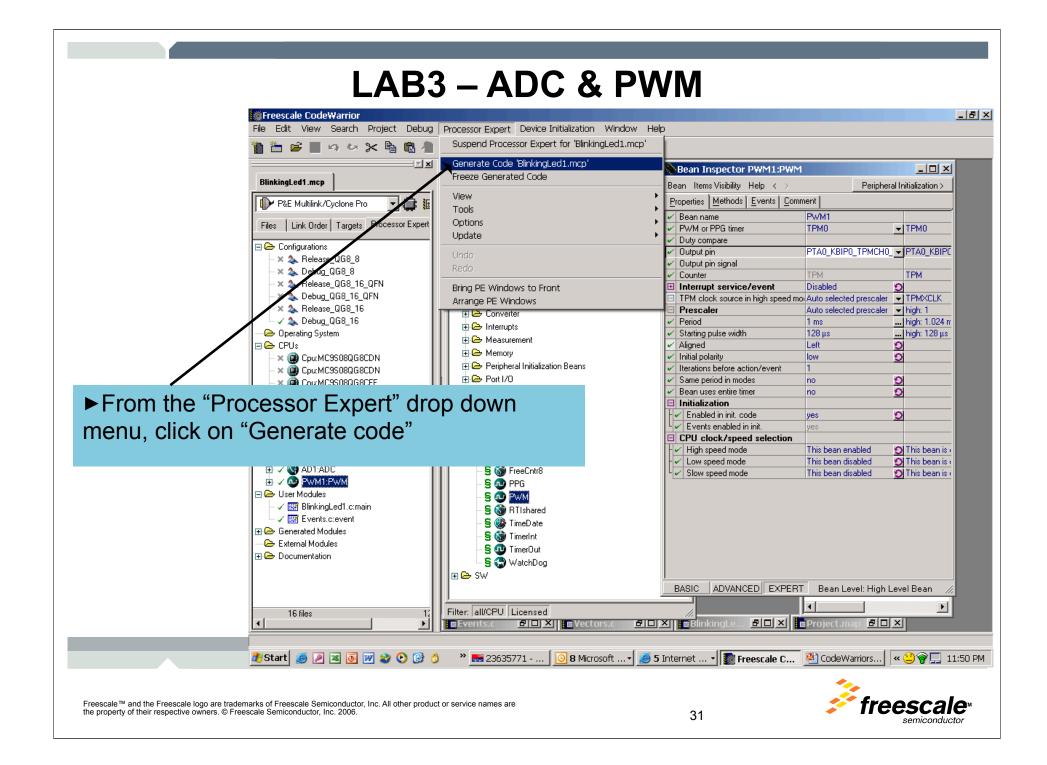
LAB3 – ADC & PWM

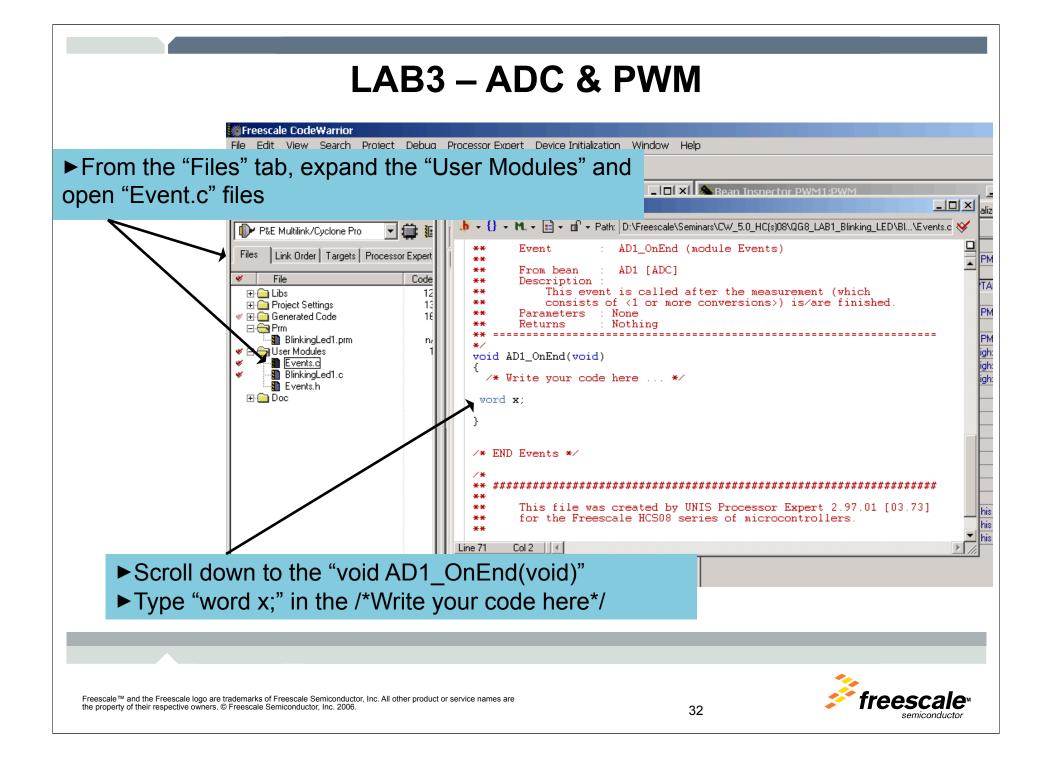


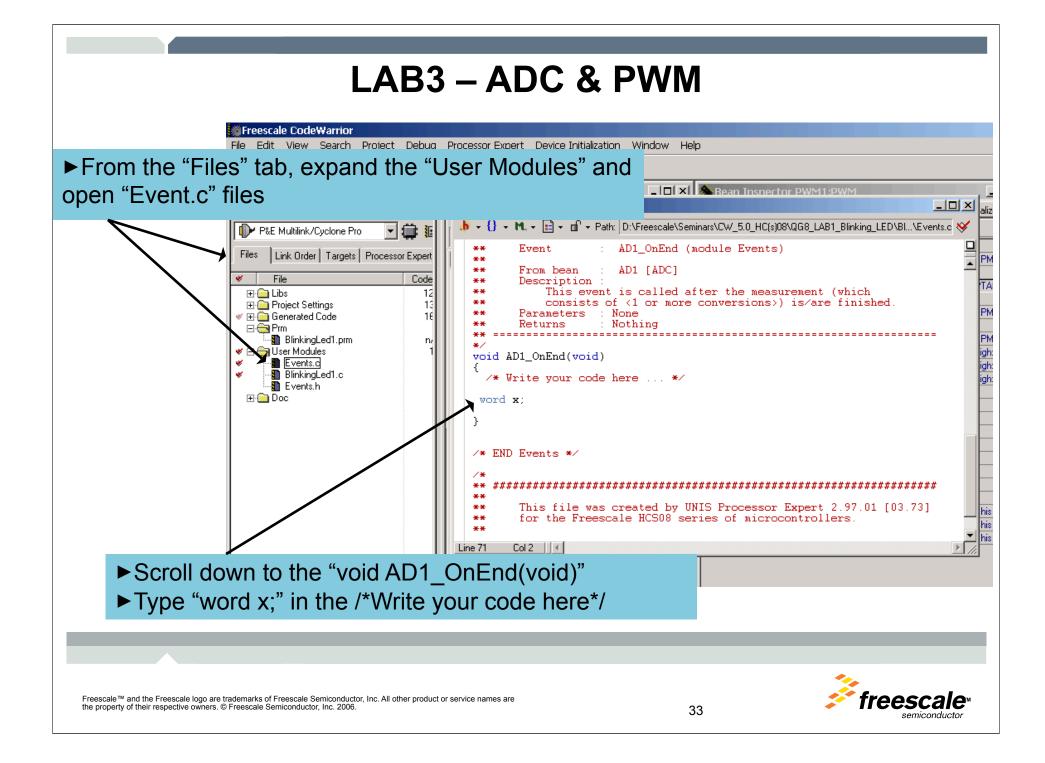
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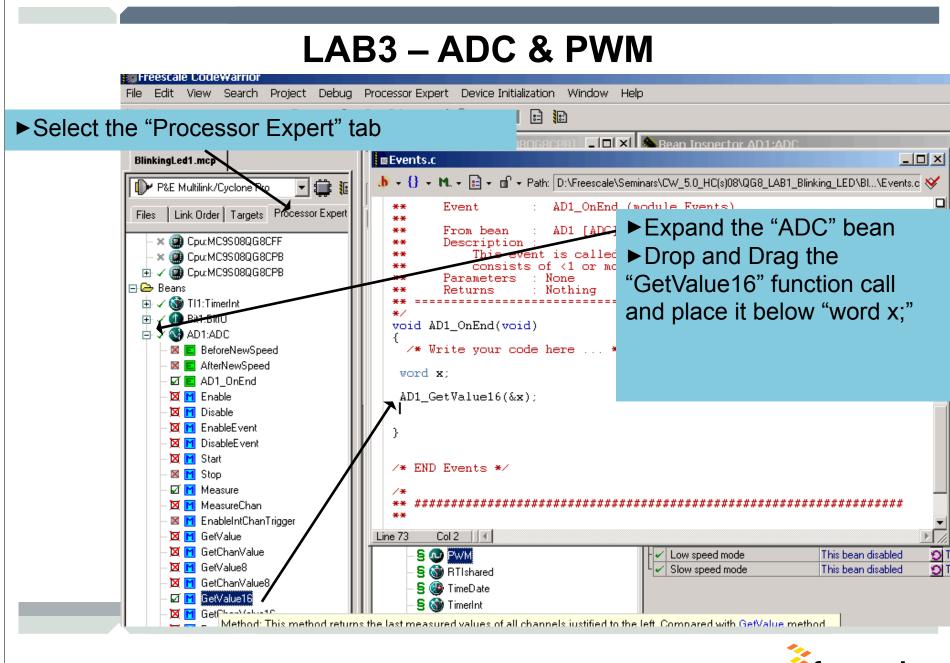


LAB3 – ADC & PWM 🚷 Bean Inspector PWM1:PWM - 🗆 × × Bean Items Visibility Help < > Peripheral Initialization > Bean Inspector PWM1:PWM - 🗆 × From the "Bean Inspector" window, click on Bean Items Visibility Help < > Peripheral Initialization > the "Period" box. Properties Methods Events Comment ► Enter "1"ms and click "OK" ► From the "Bean Inspector" window, click on 40 the "Starting Pulse Width" box. A0 KBIPC 🖌 Counter ITPM ► Enter "128" or "64" uSec and click "OK" Interrupt service/event Disabled 9 TPM clock source in high speed mo. Auto selected pre TPM Prescaler Auto selected presca high: Period Auto selected prescaler 🚽 high: not set Prescaler Starting pulse width ... Unassigned Period ...| high: 1.024 n 11 ms 9 Aligned Left high: 128 μs Starting pulse width 128 us Initial polarity low. Ð Alianed Left Ð Initial polarity low Ð Iterations before action/event 1 -Init.value Same period in modes no Э Bean uses entire timer Ð no Requested value: unit With value Units: Initialization ms. μs -ms Error allowed: unit: 🔽 % × sec Ηz % 5 kHz -Init value MHz Speed mode Adjusted value: Prescaler: Error: Xtal ticks With value Requested value: unit <u>U</u>nits: high 1.024 ms 2.4% 128 μs μs ms low disabled Error allowed: unit: 🔽 % sec Hz % 15 kHz MHz Speed Freescale ™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are freescale the property of their respective owners. © Freescale Semiconductor, Inc. 2006. 30



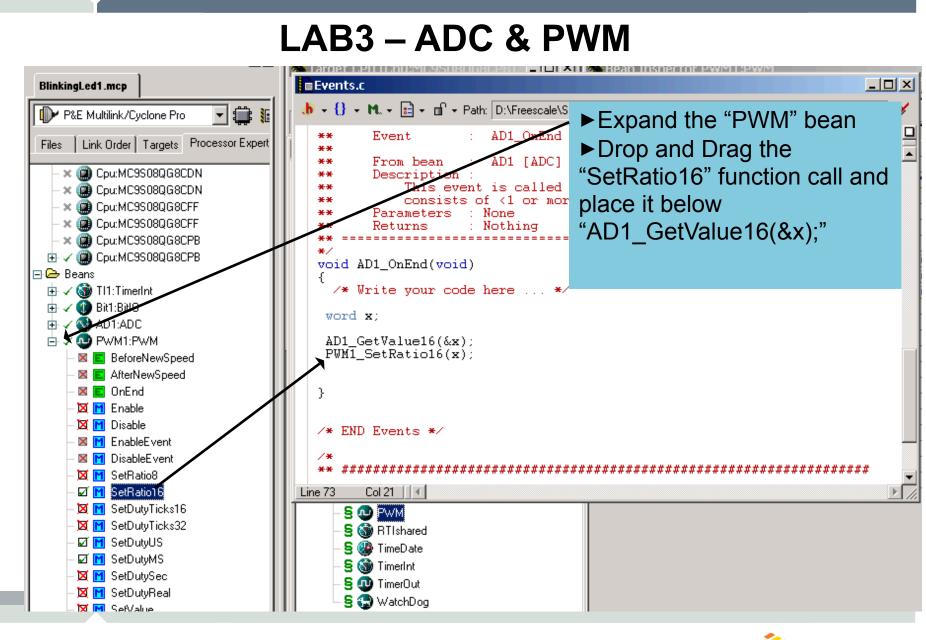






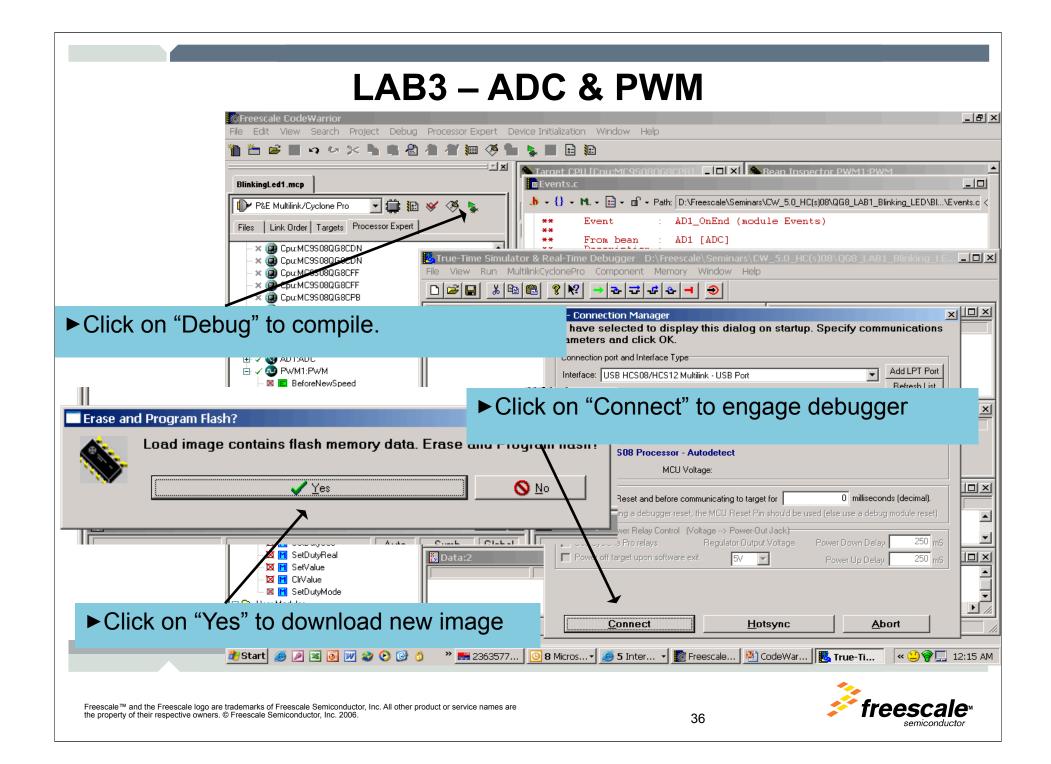
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LAB3 – ADC & PWM			
act Processor Expert Device Initialization Window Help			
A A A A A A A A A A A A A A A A A A A	0 Errors and warnings for 4	Sean Inspector PW n Items Visibility Help perties Methods Eve	
Events.c line 69	esult of function-call is ignored	Bean name PWM or PPG timer Duty compare	
	s\Condor\CLed1\HCSU8_Full_Chip_Simula Help	tor.ini	
Source Start/Continue (F5) D:\Customers\Condor\CLed1\CODE\CLed1.c #include "I0_Map h" void main(roid) { P /t** Processor Expert internal initialization. D(<u>PE low level init();</u> /*** End of Processor Expert internal initialization.		Line: 37	
 Hit "Start" icon to run the program. Roll the Thumb wheels POT on the Demo board to see the LED1 dimmed or brighten 	MODIFY THIS CODE !!! ***/		
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LAB4 – SCI Communication

Create a brand new project and set bus clk to 8Mhz.

Initialize SCI(Serial) Comm to 9600 Baud rate

Set Interrupt upon received of Character.

Set Hyperterminal on PC to 9600 baud.

Write application to echo received character back to PC



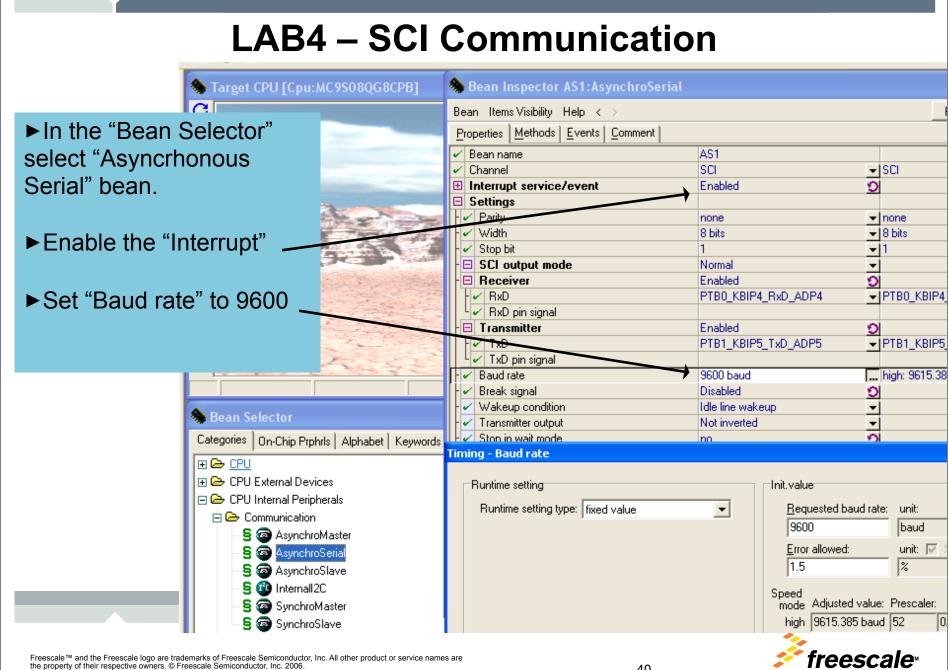
LAB4 – SCI Communication

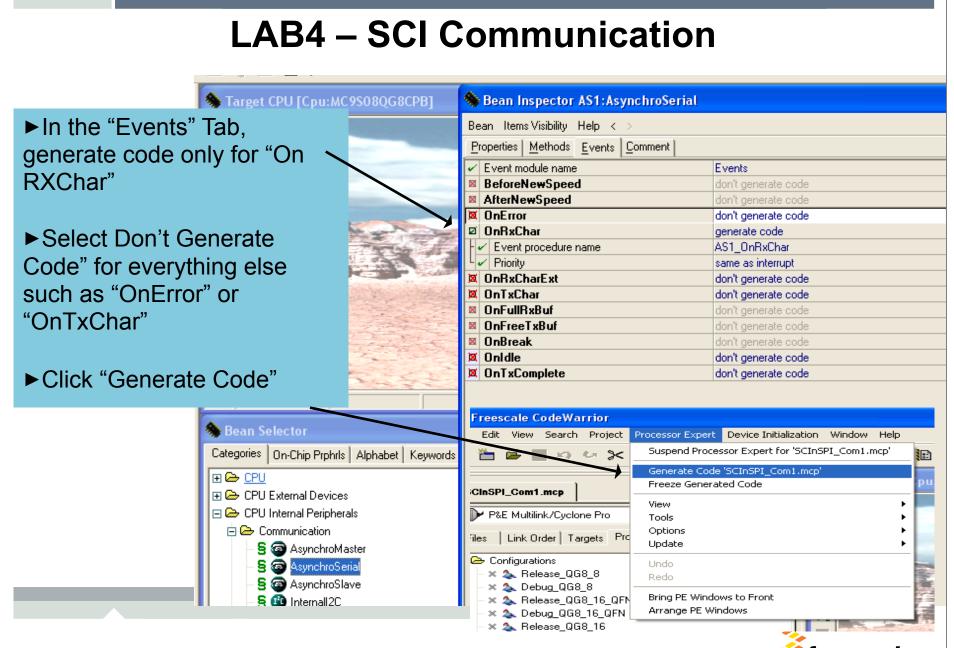
► Change the Internal Osc Frequency to 31.25Khz.

► Change the Internal BusClock to 8.0 Mhz

🚸 Bean Inspector Cpu:MC9S08QG8CPB			
Bean ItemsVisibilityHelp < >			Peripheral Initialization >
Properties Methods Events Build options U:	sed <u>C</u> omment		
✓ Bean name	Сри		~
CPU type	MC9S08QG8CPB	-	
Clock settings			
E Internal clock			
- 🗸 Internal oscillator frequency [kHz]	31.25	31.25 kHz	
🛛 🗆 Initialize trim value	yes	0	
- 🗸 Trim value address	FFAF	н	
└ ✔ Fine trim value address	FFAE	н	
External clock	Disabled 🖸		
LE Low-power modes settings			
L STOP instruction enabled	no	▼	
Initialization interrupt priority	interrupts enabled	<u>▼</u> 1	
	nis property enables the STOP instruc	tion.	
□ High speed mode	Enabled		
	Internal Clock	▼ 31.25 kHz	
- Bus freq. divider	Auto select	▼ 1	
- 🗸 Internal bus clock	8.0	8.0 MHz	
Fixed freq. clock clk src.	Divided FLL reference clock		
 Fixed frequency clock 	0.015625	0.0156251	MHz
E FLL mode	Engaged	-	



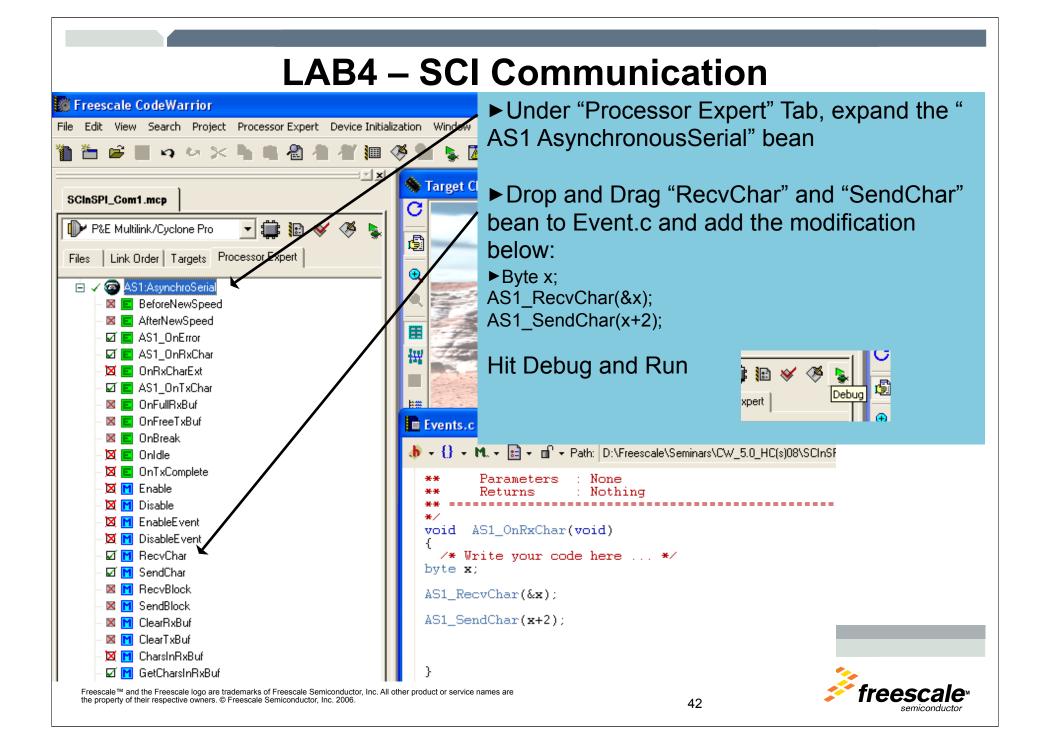


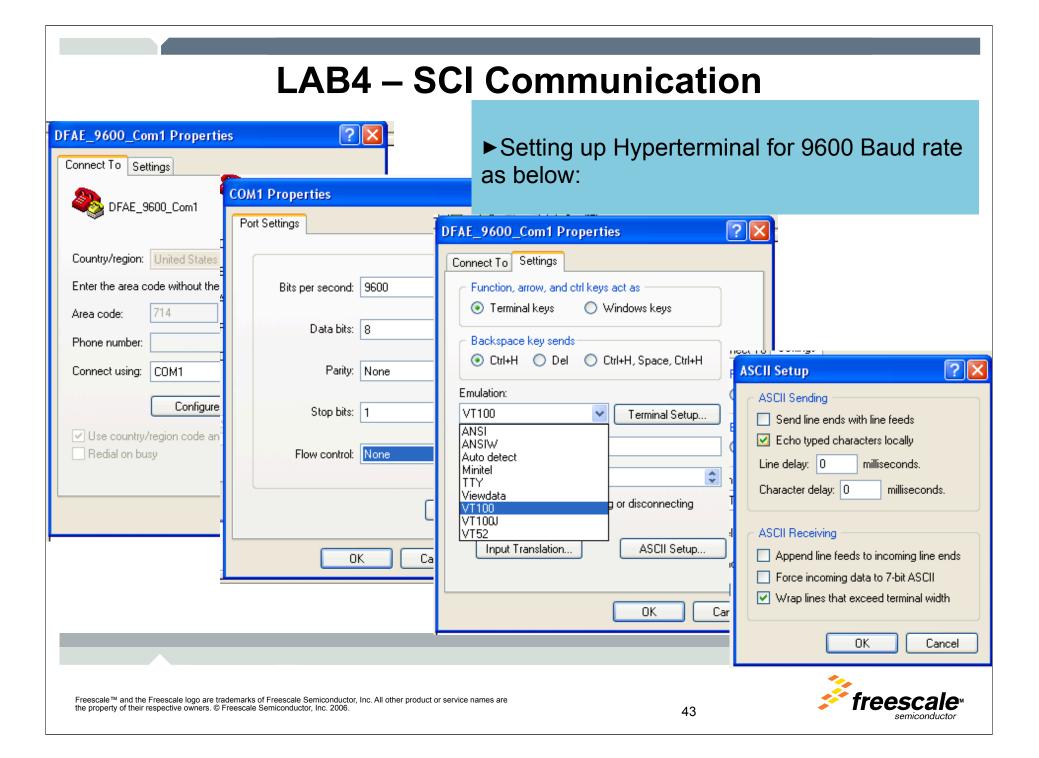


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LAB5 – SPI Communication

► To send communication from PC to PC via an QG8 SCI/SPI converter

- ► Continuation with LAB4 (SCI Comm).
- ► Initialize SPI for MasterMode
- ► Initialize SPI for Slave Mode
- ► Write SCI/SPI Converter code
- ► Use Hyperterminal to test and application.



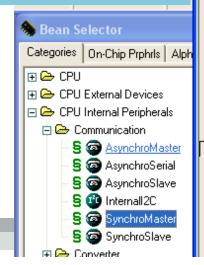
LAB5 – SPI Communication(Master)

SPI Master Configuration

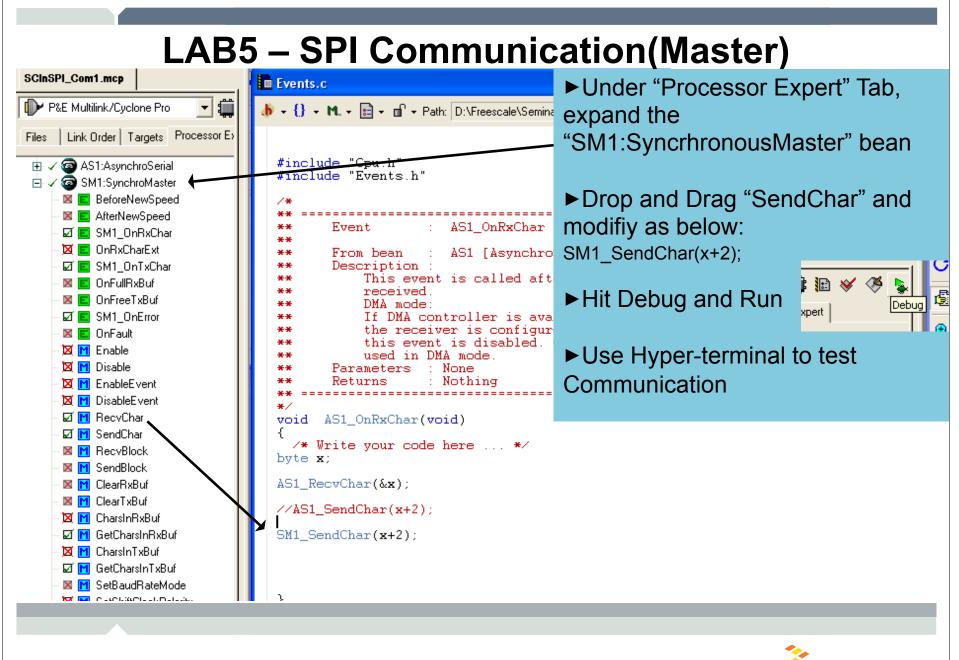
► In the "Bean Selector" window, select Synchronous Master.

Enable "Slave Select pin" and set Direction to Output

► Set "Clock rate" to 4Mhz



Bean Items Visibility Help < >Peri Properties Methods Events Comment	Sean Inspector SM1:SynchroMaster				
Properties Methods Events Comment ✓ Bean name SM1 ✓ Channel SPI SPI Interrupt service/event Enabled O ✓ Interrupt service/event Enabled O ✓ Interrupt from input Vspi Vspi ✓ Interrupt input priority medium priority Interrupt not supported ✓ Interrupt from output medium priority peripheral does not support interrupt ✓ Interrupt output priority medium priority peripheral does not support interrupt ✓ Interrupt from output peripheral does not support interrupt ✓ Interrupt from output peripheral does not support interrupt ✓ Interrupt from output peripheral does not support interrupt ✓ Interrupt from output peripheral does not support interrupt ✓ Interrupt from output peripheral does not support interrupt ✓ Interrupt interrupt D O ✓ Prin PTB4_MISO PTB4_MISO PTB4_MISO			Peri		
✓ Bean name SM1 ✓ Channel SPI ▼ SPI Interrupt service/event Enabled ♥ ✓ Interrupt from input ✓ ✓ Interrupt from input ✓ ✓ Interrupt from output ✓ ✓ Interrupt from output ✓ ✓ Interrupt from output ✓ ✓ Interrupt output priority medium priority ✓ ✓ Interrupt from output ● Peripheral does not support interrupt ✓ Interrupt from output ● Peripheral does not support interrupt ✓ Interrupt from output ● Peripheral does not support interrupt ✓ Interrupt from output ● Peripheral does not support interrupt ✓ Prin signal ● ● Peripheral does not support interrupt ✓ Prin signal ● ●					
✓ Channel SPI ▼ SPI Interrupt service/event Enabled Q ✓ Interrupt from input Vspi Vspi ✓ Interrupt from input medium priority ▼ not supported ✓ Interrupt input priority medium priority ▼ not supported ✓ Interrupt output priority medium priority ▼ peripheral does not support interrupt ✓ Interrupt output priority medium priority ▼ peripheral does not support interrupt ✓ Interrupt output priority medium priority ▼ peripheral does not support interrupt ✓ Interrupt output priority medium priority ▼ peripheral does not support interrupt ✓ Input buffer size 0 0 ✓ Output buffer size 0 0 ✓ Pins ignal Q PTB4_MISO PTB4_MISO ✓ Pin signal PTB3_KBIP7_MOSI_ADP7 PTB3_KBIP6_SPSCK_ADP6 ✓ Pin signal Q PTB5_TPMCH1_SS PTB5_TPMCH1_SS ✓ Pin signal Q Q PTB5_TPMCH1_SS PTB5_TPMCH1_SS ✓ <t< td=""><td></td><td>1</td><td></td></t<>		1			
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✓ Output buffer size 0 ✓ Britectional mode Disabled ✓ Pin Enabled ✓ Pin PTB4_MISO ✓ Pin signal ✓ ✓ Direction Output ✓ ✓ Shift clock rate 4 MHz			peripheral does not support interrupt		
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Output pin Enabled Image: Coordination of the second		PTB4_MISO -	PTB4_MISO		
Image: State of the state					
✓ Pin signal PTB2_KBIP6_SPSCK_ADP6 PTB2_KBIP6_SPSCK_ADP6 ✓ Pin signal Enabled ✓ ✓ Pin signal ✓ PTB5_TPMCH1_SS PTB5_TPMCH1_SS ✓ Pin signal ✓ Output ✓ ✓ Direction Output ✓ ✓ ✓ Clock edge rising or falling edge ✓ rising edge ✓ Shift clock rate 4 MHz … high: 4 MHz ✓ Ignore empty char. no ✓ ✓ Shift clock idle polarity Low ✓		· · · · · · · · · · · · · · · · · · ·			
Clock pin PTB2_KBIP6_SPSCK_ADP6 PTB2_KBIP6_SPSCK_ADP6 Pin signal Enabled PTB5_TPMCH1_SS Pin signal PTB5_TPMCH1_SS PTB5_TPMCH1_SS Pin signal Output Image: Space select pin Image: Space select pin Pin signal Output Image: Space select pin Image: Space select pin Image: Space select pin Pin signal Output Image: Space select pin Image: Space select pin Image: Space select pin Pin signal Output Image: Space select pin Image: Space select pin Image: Space select pin Pin signal Output Image: Space select pin Image: Space select pin Image: Space select pin Pin signal Output Image: Space select pin Image: Space select pin Image: Space select pin Pin signal Output Image: Space select pin Image: Space select pin Image: Space select pin Pin signal Output Image: Space select pin Image: Space select pin Image: Space select pin Pin signal Image: Space select pin Image: Space select pin Image: Space select pin Image: Space select pin Image: Space select pin Image: Space select p		PTB3_KBIP7_MOSI_ADP7	PTB3_KBIP7_MOSI_ADP7		
✓ Pin PTB2_KBIP6_SPSCK_ADP6 ✓ PTB2_KBIP6_SPSCK_ADP6 ✓ Pin signal Enabled Ø ✓ Pin PTB5_TPMCH1_SS ✓ PTB5_TPMCH1_SS ✓ Direction Output ✓ ✓ Clock edge rising or falling edge ✓ rising edge ✓ Shift clock rate 4 MHz high: 4 MHz ✓ Ignore empty char. 0 Ø ✓ Send MSB first no Ø ✓ Shift clock idle polarity Low ✓					
✓ Pin signal ✓ Pin ✓ Pin ✓ Pin signal ✓ Pin signal ✓ Direction ✓ Clock edge ✓ Shift clock rate ✓ Shift clock rate ✓ Ignore empty char. ✓ Send MSB first ✓ Shift clock idle polarity					
Slave select pin Enabled O Pin PTB5_TPMCH1_SS PTB5_TPMCH1_SS Pin signal Output Image: Specific stress of the stress of th		PTB2_KBIP6_SPSCK_ADP6	PTB2_KBIP6_SPSCK_ADP6		
Pin PTB5_TPMCH1_SS PTB5_TPMCH1_SS Pin signal Output Image: Shift clock rate Image: Shift clock rate Shift clock rate 4 MHz Image: Shift clock rate Image: Shift clock rate Image: Shift clock rate 0 Image: Shift clock rate Image: Shift clock rate Image: Shift clock rate 0 Image: Shift clock rate Image: Shift clock rate Image: Shift clock rate 0 Image: Shift clock rate Image: Shift clock rate Image: Shift clock rate 0 Image: Shift clock rate Image: Shift clock rate Image: Shift clock rate 0 Image: Shift clock rate Image: Shift clock rate Image: Shift clock rate 0 Image: Shift clock rate Image: Shift clock rate Image: Shift clock rate 0 Image: Shift clock rate Image: Shift clock rate Image: Shift clock rate 0 Image: Shift clock rate Image: Shift clock rate Image: Shift clock rate 0 Image: Shift clock rate Image: Shift clock rate Image: Shift clock rate 0 Image: Shift clock rate Image: Shift clock rate Image: Shift clock rate 0 Image: Shift clock rate <					
✓ Pin signal ✓ Direction ✓ Direction ✓ Clock edge ✓ Shift clock rate ✓ Shift clock rate ✓ Empty character ✓ Ignore empty char. ✓ Send MSB first ✓ Shift clock idle polarity					
✓ Direction Output ✓ Clock edge rising or falling edge ✓ Shift clock rate 4 MHz ✓ Empty character 0 ✓ Ignore empty char. no ✓ Send MSB first no ✓ Shift clock idle polarity Low		PTB5_TPMCH1_SS	PTB5_TPMCH1_SS		
✓ Clock edge rising or falling edge ✓ rising edge ✓ Shift clock rate 4 MHz high: 4 MHz ✓ Empty character 0 ✓ Ignore empty char. no O ✓ Send MSB first no O ✓ Shift clock idle polarity Low ✓					
Image: Shift clock rate 4 MHz Image: MHz Image: Shift clock rate 0					
Ignore empty char. 0 Ignore empty char. no Send MSB first no Shift clock idle polarity Low	-				
✓ Ignore empty char. no O ✓ Send MSB first no O ✓ Shift clock idle polarity Low ✓		4 MHz	high: 4 MHz		
✓ Send MSB first no ✓ Shift clock idle polarity Low		-			
✓ Send MSB first no ✓ Shift clock idle polarity Low		no 🖸			
		no 🖸			
	- 🖌 Shift clock idle polarity	Low 👻			
		N 11 1	* <u>*</u>		



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LAB5 – SPI Communication(Slave)

SPI Slave Configuration

► In the "Bean Selector" window, select SynchronousSlave.

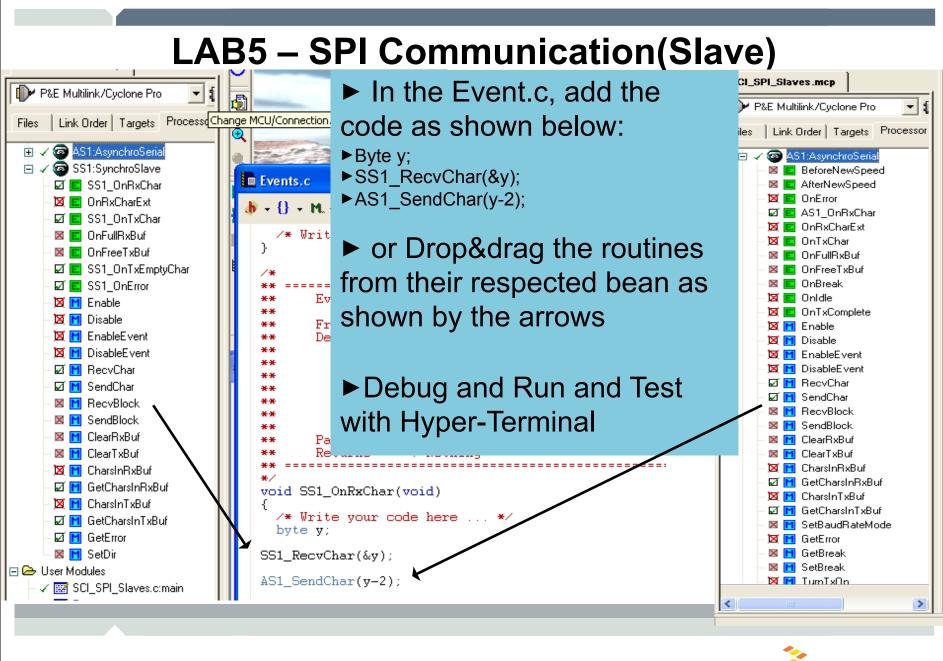
► Set "Clock Edge" to rising edge to match up with the Master mode.

► Generate Code

🔦 Bean Selector		
Categories	On-Chip Prphrls	Alphabet
🕀 🗁 CPU		
🕀 🗁 CPU	External Devices	
🕞 🗁 CPU Internal Peripherals		
🛛 🖻 🗁 Co	ommunication	
-9	o AsynchroMa	ster
-9	AsynchroSer	ial
-9	AsynchroSla [®]	ve
-9	Internall2C	
-9	SynchroMasl	ter
_ <u>-</u> S	SynchroSlav	e
	Categories	Categories On-Chip Prphrls

Bean Inspector SS1:SynchroSlave			
Bean ItemsVisibilityHelp < >			Peripheral Initialization
Properties Methods Events Comment			
🗸 Channel	SPI	-	SPI
Interrupt service/event	Enabled	9	
- 🖌 Interrupt	Vspi		Vspi
V Interrupt from input			
V Interrupt input priority	medium priority	_	not supported
V Interrupt from output			
 ✓ Interrupt output priority 	medium priority	-	peripheral does not suppor
- 🗸 Input buffer size	0		
└/✔/ Output buffer size	0		
Settings			
- Ridirectional mode	Disabled	9	
	Enabled	9	
- 🗸 Pin	PTB3_KBIP7_MOSI_ADP7	-	PTB3_KBIP7_MOSI_ADP
🗸 🖌 Pin signal			
🗉 Output pin	Enabled	9	
Pin Pin	PTB4_MISO	-	PTB4_MISO
🛛 🗸 Pin signal			
🗆 Clock pin			
Pin Pin	PTB2_KBIP6_SPSCK_ADP6	-	PTB2_KBIP6_SPSCK_AD
🗸 🖌 Pin signal			
🗉 Slave select pin	Enabled	9	
Pin Pin	PTB5_TPMCH1_55		PTB5_TPMCH1_SS
🛛 🗸 Pin signal			
🖌 Clock edge	rising or falling edge	-	rising edge
 Empty character 	0		
✓ Ignore empty char.	no	9	
Send MSB first	no	ວ ວ •	
Shift clock idle polarity	Low	-	
Stop in wait mode	no	0	
Initialization			

semiconductor



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LAB6 – I2C Communication

► Modify HW to add 4.7K resistors to SCL and SDA signals

► Initialize I2C HW

► Write I2C application



LAB6 – I2C Communication			
I2C_help.mcp P&E Multilink/Cyclone Pro Files Link Order Targets Proc	Target CPU [Cpu:MC9S08] Bean Inspector I2C1:InternalI2C Bean Items Visibility Help < > Properties Methods Events Comment Image: Comment Image: Comment Image: Comment Image:	Modify I2C Bean Configuration as below:	
☐ Configurations — ×	€ ✓ I2C channel ✓ Mode selection □ □ Interrupt service/event ✓ ✓ Interrupt ✓	IIC ▼ IIC MASTER - SLAVE ▼ Enabled Viic	
 × Selease_QG8_16_QFN × Debug_QG8_16_QFN × Selease_QG8_16 ✓ Debug_QG8_16 ✓ Debug_QG8_16 		medium priority Init supported Enabled 8 8 8 Enabled 8 Enabled 8	
CPUs CPUs Cpu:MC9S08QG8CDN Cpu:MC9S08QG8CDN Cpu:MC9S08QG8CDN Cpu:MC9S08QG8CFF	Polling trials Automatic stop condition Initialization Slave address init	2000 yes 🕥 8 🛛	
	signal GND Slave address Bean Selector Categories On-Chip Prphrls Alpha	Enabled C Disabled C D C D C D C D C D C D C D C D C D C	
 ✓ ⁽¹⁾ I2C1:Internall2C ✓ User Modules ✓ (12C_help.c:main ✓ (12C_help.c:event 		PTB6_SDA_XTAL PTB7_SCL_EXTAL PTB7_SCL_EXTAL PTB7_SCL_EXTAL	
■ Generated Modules — External Modules — Documentation	-Sigo AsynchroMaster -Sigo AsynchroSerial -Sigo AsynchroSerial -Sigo AsynchroSerial -Sigo AsynchroSlave -Sic SCL frequency	8 MHz high: 8 MHz 000	
	Structure Structure Structure Structure Structure Structure Initialization Structure Structure Structure Structure Structure Structure Structure Structure Structure Structure Structure S	yes O	

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LAB6 – I2C Communication

Right hand click on "Internal I2c" bean and File Folder 911302006 1118 PM 🐸 Processor Expert - Mozilla Firefox _ 🗆 X select Help on Bean from Bookmarks Tools Edit View Go File Help Drop down menu. O Go G 2 📄 file:///D:/Program%20Fi 💌 Select Typical Usage X Processor Expert Processor Expert 🗞 Bean Selector Processor Expert with Embedded Bea Categories On-Chip Prphrls | Alphabet | Keywords | Quick help > 🕞 🗁 CPU Embedded Beans CPU Beans Processor Expert OnLine 🕀 🗁 CPU External Devices 🖃 🗁 CPU Internal Peripherals Bean InternalI2C InternalI2C 🖻 🗁 Communication Internal I2C Communication Interface 🧧 🖾 AsynchroMaster General Info 🧧 🚳 AsynchroSerial Level: High Level Bean Category: CPU Internal Peripherals-Communication roperties 🗧 🕝 AsynchroSlave S 🙂 Internall2C Methods. This bean encapsulates the internal I2C communication Events Add Bean to the Current Project 🧧 🔕 SynchroM interface. The implementation of the interface is based on Typical Usage 🧧 🚳 SynchroSk Delete Selected Template the Philips I2C-bus specification. Interface features: 🕀 🗁 Converter Help on Bean 🗄 🗁 Interrupts MASTER mode Help on Bean Selector 🛨 🗁 Measurement Types & definitions × . 🗄 🗁 Memory Multi master communication Embedded Beans The combined format of communication nossible > Done 🕑 💧 æ 🕒 4 Microsoft Office ... Reescale CodeWarrior Microsoft PowerPoin... 😻 Processor Expert - M... 🛅 3 Windows Explorer Freescale ™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are reesc the property of their respective owners. © Freescale Semiconductor, Inc. 2006 51

LAB6 – I2C Communication

🐸 Processor Expert	- Mozilla Firefox	HomeWork:
<u> Eile E</u> dit <u>V</u> iew <u>G</u> o	Bookmarks Tools Help	
Processor Expert	file:///D:/Program%20Files/Freescale/CodeWarrior%20for%20HC08% Processor Expert Processor Expert with Embedded Beans	using the Typical Usage Help Menu
	Embedded Beans CPU Beans Processor Expert OnLine	Remember to add 4.7k resistors
v	Interrupt handler code in the bean	to SDA and SCL line before calling He My FAE.
	User application code in the event module, typically called from t	
	I2C peripheral module sends or receives a byte	
	Call of a method or occurence of an event	
	Return from a method, event or interrupt	
	 Typical settings and usage of InternalI2C bean (1) Sending data in the MASTER mode (2) Receiving data in the MASTER mode (3) Sending data in the SLAVE mode (4) Receiving data in the SLAVE mode (5) Sending data in the MASTER mode without interrupts (6) Receiving data in the MASTER mode without interrupt 	
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CodeWarriors & Processor Expert Seminar

Thank You

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